ENERGY RECOVERY FLIP-FLOPS AND RESONANT CLOCKING OF SCCER FLIP-FLOP IN H-TREE CLOCK NETWORK

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Abstract: This paper indicates the four novel low power flip-flops collectively called novel energy recovery flip-flops to reduce the power dissipation in a clock network. The energy recovery clocked flip-flops enable energy recovery from the clock network, resulting in significant energy saving. The designed flip-flop operates with a single phase sinusoidal clock generated by an efficient power clock generator. A multiplier of 2 × 2 bit pipelined in 3 stages is designed. The schematic of the synthesized net list is generated and simulation results are presented for general D flip-flop and after replacing them by the designed SCCER flip-flop. The results show 43.56 % less power dissipation in compare to normal D flip-flop. In order to demonstrate the feasibility of energy recovery clocking, we integrated 64 energy recovery SCCER clocked flip-flops distributed across an area of 1 mm × 1 mm and clocked them by a single-phase sinusoidal clock through an 4 levels deep H- tree clock network. We report here that in H tree based clock network there is 90% of energy recovery for SCCER flip-flop over conventional flip-flop (HLFF).

Key words: energy recovery; flip-flops; clock; clock network; CMOS digital integrated circuits; sinusoidal clock.

I. INTRODUCTION

Flip-flops are presented everywhere in CMOS circuits based designs which make the major portion of the synchronous circuits. As a result, the structure of flip-flop used in circuits has a large impact on system power consumption. Moreover, the type of flip-flop used determines the amount of clock load, which directly affects dynamic power consumption PDYN of a circuit. Thus, it is prudent to come up with techniques to reduce the overall system power consumption [13]. A number of low PDP based pulse triggered flip-flops were also designed from time to time [6, 8, 11]. It was observed that the power dissipated in Clock Distribution Network (CDN) is 30% to 60% of the total system power, where 90% of which is consumed by the flip-flop

and the CDN that is driving the flip-flops [9]. The major fraction of the total power consumption in highly synchronous designs such as microprocessors is due to the clock network. In the Xeon Dual-core processor, a significant portion of the total chip power is due to the CDN [18]. Thus, innovative clocking techniques for lowering the power consumption of the clock networks are required for future high performance and low power designs. As the power budget of today's portable digital circuit is severely limited, it is important to reduce the power dissipation in both CDN and in the flip-flops. Resonant clocking is an attractive alternative to conventional clock distribution due to its significant potential for reducing clocking power [7]. Typically, resonant clock systems rely on sinusoidal clock signals to synchronize the flip-flops. The scheme of energy recovery clocking was used by many people to achieve ultra low power [3, 12]. Here we apply the energy recovery techniques to clock network since the clock signal is typically the most capacitive signal in a chip. The designed energy recovery clocking scheme recycles the energy from this capacitance in each cycle of the clock. For an efficient clock generation, we have used a sinusoidal power clock signal generator.

II. MECHANISM, TIMING DEFINITION AND TOOLS USED

1. MECHANISM

Adiabatic logic is also called energy recovery logic. Instead of dissipating the power these logic reuse it. Energy recovery is the promising techniques designed by adiabatic logic and consumes less power over conventional CMOS based logic [19]. It achieves low power consumption by restricting the currents to flow across devices with low voltage and

by recycling the energy stored in their node capacitors using an AC type power supply rather than DC [1, 12].
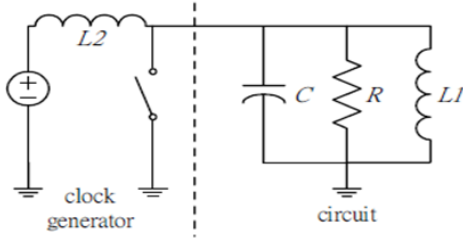

Figure 1. General Principle of resonant clocking [2].

In conventional clock design clock buffers are used to amplify and to balance the clock skew. Like conventional clock network energy-recovery clock networks do not use any buffers. Power consumption in conventional clock distribution is proportional to CV^2, where C is the total switched capacitance and V is the difference between power and ground voltages, while on the other hand the energy consumption in charge recovery logic scales with $\frac{RC}{T}(CV^2)$ [1, 4]. A simple model of a resonant clocked system is shown here [Figure 1]. Here power clock generator fills again the energy losses of the system and maintained the amplitude of oscillation in resonant mode. The parameters R and C are equivalent load and capacitance of the circuit. The parameter L1 is the equivalent inductance of interconnects, and the parameter L2 is an inductive element of the power-clock generator [2].

2. TIMING, TOOLS AND TECHNOLOGY USED

Figure 2 represents the timing definition for all the observations. We considered the reference point for all the observations in rising edge of the clock from half of the supply voltage. The figure 3 represents the timing requirements to send the correct data at output. Set up time is defined as the time from when the data is stable before the rising edge of the clock [16].

$$T_{CLK} \geq T_{CLK-Q} + T_{logic} + T_{su} \qquad (1)$$

It imposes extra constraint for proper operation. Hold time is defined as the time from the rising transition of clock to the earliest time when data may change after being sampled [16].

$T_{hold} \leq T_{CDreg1} + T_{CDlogic}$
From figure 2 hold time will be negative and large,

since the data is held before the clock edge. The CLK-Q delay is defined as the time from 50% of the rising edge of the CLK to the more delayed output (here QB) to verify the timing definition [12]. The D-Q delay is defined as time from the point where D transition reaches 50% of the supply voltage to the point where the Q transition reaches 50% of the supply voltage. We simulate the designs with MENTOR GRAPHICS Design Architect (DA) Tool in 0.25 μm technology with a supply voltage of 2.5V. The design was optimized at temperature of 27˚C for a single phase sinusoidal clock with 200 MHz frequency and a load capacitance of 30 fF was used in the output side. The designs were laid out using MENTOR GRAPHICS IC station. Net list with parasitic capacitance were extracted and simulated to verify the design. To simulate the verilog code Model Sim-Altera web addition 6.3g_p1 is used. For synthesizing the code Mentor Graphics Leonardo- Spectrum tool is used.
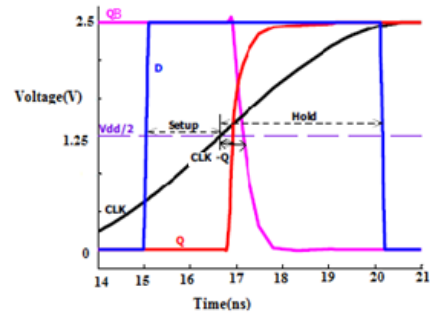

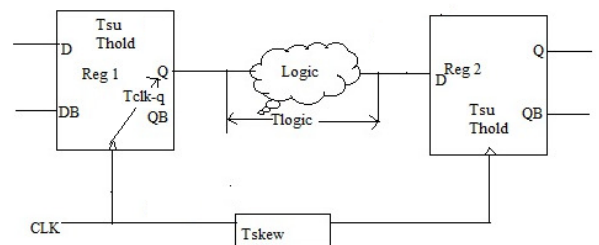Figure 2. Sample waveforms for timing definition [12].

Figure 3. Timing requirements.

III. ENERGY RECOVERY CLOCKED FLIP-FLOPS

In this section we have discussed on the four energy recovery flip-flops and conventional energy recovery clocked flip-flops [3]. The flip-flops that operate with square wave clocking are hybrid latch flip-flop (HLFF) [15], conditional capturing flip-flop (CCFF) (Kong et al., 2002) and transmission gate flip-flop (TGFF) [10]. HLFF and CCFF are high speed flip-flop. Four phase transmission gate

(2)

(FPTG) flip-flop is also the conventional energy recovery flip-flop [20]. It is same as conventional transmission gate flip-flop (TGFF) except that it uses four pass transistor gates to conduct for a short fraction of clock period [14]. TGFF is a low power flip-flop. Here in our case we are considering HLFF as a conventional flip-flop. All the flip-flops are laid out and .PEX net list is generated after parasitic extraction. Post layout simulation results are also matched for each flip-flop.

1. SENSE AMPLIFIER ENERGY RECOVERY FLIP-FLOP (SAER)

These flip-flops are dynamic flip-flop with precharge and evaluate phases of operation [14]. This flip-flop is used as an energy recovery flip-flop to recover the energy from clock distribution network and clock input capacitance of flip-flops [12]. Due to slow rising /falling transition of the clock signal there is the possibility of short circuit in the storage elements during recovering the energy from clock distribution network. This flip-flop can also be used to operate with the low voltage swing clock [9]. The figure 4 represents the schematic of sense-amplifier based flip-flop.
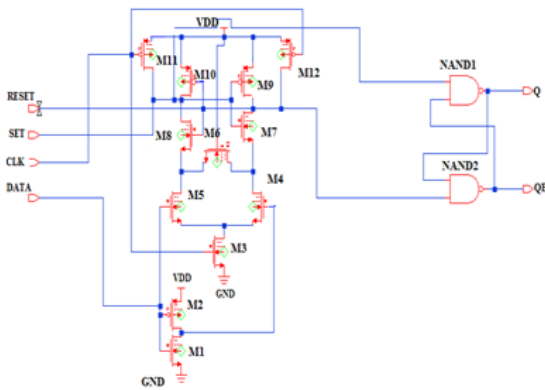

Figure 4. Schematic of SAER flip-flop.

Since it is a dynamic flip-flop it has two phases of operations precharge and evaluation.

(i) Precharge phase- when the CLK transits from H → L, M11 and M12 precharge transistor will be off initially and will become on as CLK reaches VDD – Vtp, where Vtp is the threshold potential of M11 and M12. From fig. 5 when SET is high and RESET changes, the output of feedback cross coupled inverter (Q and QB) maintain its state.

(ii) Evaluation phase-When the clock transits L → H, initially M3 is off and as CLK voltage exceeds the threshold voltage (Vtn) of M3 the evaluation occurs. In this phase the difference between (DATA (D) and DATAB (DB) result in small voltage difference between set and reset nodes which is amplified by cross coupled inverter and as a result either set or reset node switches to low. When M3 and M5 are on, SET node will be discharge through three stacked NMOS series transistors M3, M5 and M8, that causes output Q to charge to 1, while RESET node is high. This state transition is captured by the SET/RESET latch (made of NAND gates) and retained for the rest of the cycle time until the next evaluation occurs as shown in fig 5.
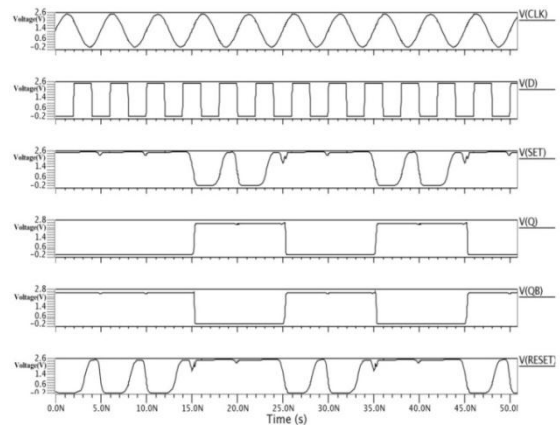

Figure 5. Simulated output of conventional SAER flip-flop.

SAFF has delay penalty due to two reasons: first the use of three stacked NMOS transistors and second due to low speed of static output latch. The SAFF performs very well in terms of power dissipation and high data switching activity due to minimum sizing and stacking effect [15]. From fig. 5 it is clear that SET and RESET node always charge to VDD and discharge regardless of data input condition. The use of M6 transistor is to provide the DC leakage path for both SET/RESET nodes to ground. Consequently internal nodes charge/discharge regardless of input condition (Fig. 5). The total power consumption can be significantly reduced by avoiding such redundant internal switching [13]. The figs. 5 and 6 represent the simulated output and layout of SAER flip-flop respectively. It is a critical issue with low data switching activity. To overcome that two approaches are presented [3] –

(i)   Static flip-flop (SDER)
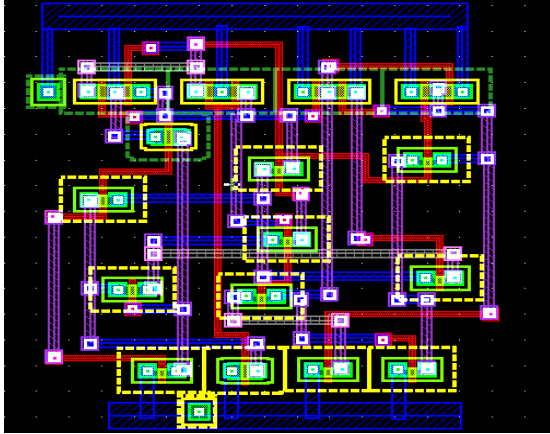(ii)   Conditional captured flip-flop (DCCER and SCCER)
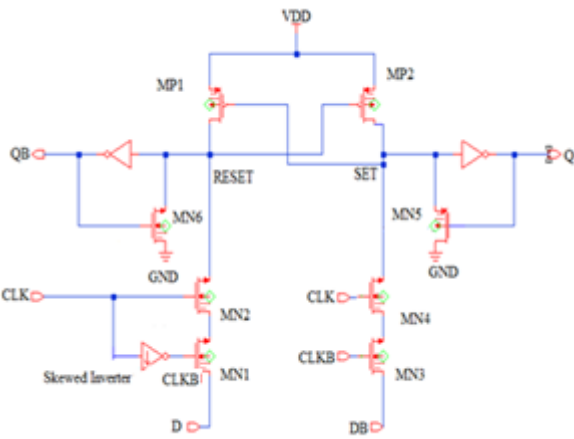

Figure 6. Layout of SAER flip-flop.

Figure 7. Schematic of SDER flip-flop.

2.   STATIC DIFFERENTIAL ENERGY RECOVERY FLIP-FLOP (SDER)

The schematic of SDER flip-flop is presented in fig. 7. This flip-flop is dual-rail static edge-triggered latch (DSETL) and is static in nature [5]. The static nature is due to SET and RESET nodes, those statically retains the state of the flip-flop. The minimum sized inverter skewed for fast H → L transition creates a sharp H → L transition on CLKB to ensure correct timing for the flip-flop operation. The role of minimum sized skewed inverter is to ensure correct timing for the flip-flop operation. The minimum sizing of the inverter also help to reduce the short circuit power. The CLK signal and the skewed CLKB are applied to transistors MN2 and

MN1 (MN4 and MN3). The series combination of these nMOS transistors MN2 and MN1 (MN4 and MN3) open for a short time when both for CLK and CLKB have voltages above the threshold voltages. Here the conducting pulse is generated during each rising transition of the clock since the inverter is skewed for sharp H → L transition. A cascade of three inverters instead of one can give a slightly sharper falling edge for the inverted clock (CLKB) as was used in DSETL latch [5].
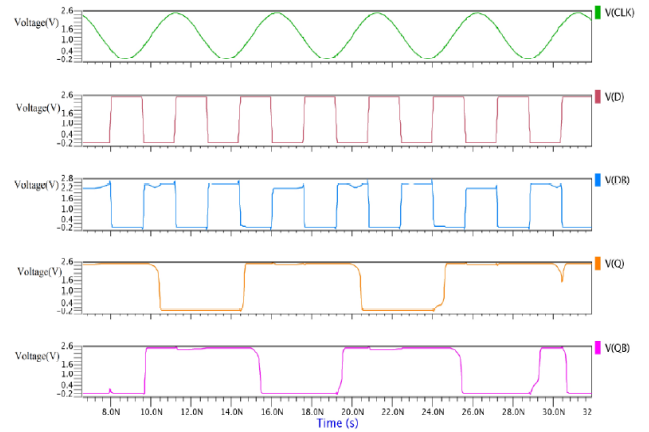

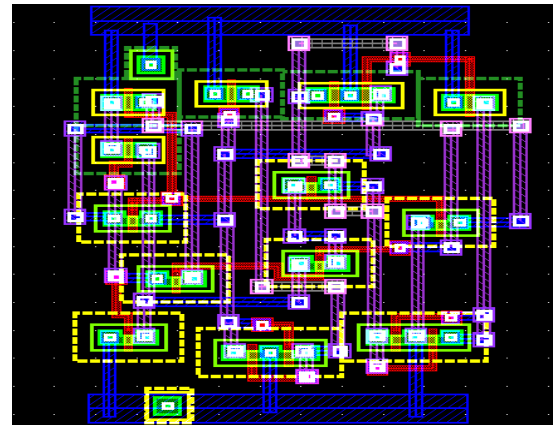Figure 8. Simulated output of SDER flip-flop.

Fiure 9. Layout of SDER flip-flop.

The advantage of SDER over SAER ensures that there is no internal redundant switching on SET and RESET nodes if input data remains idle for long time. Therefore, power consumption is minimized for low data switching activities. The following figure 8 represents the simulated output of SDER. Figure 9 represents the layout of SDER.

3. DIFFERENTIAL CONDITIONAL CAPTURE ENERGY RECOVERY FLIP-FLOP (DCCER)

The second approach for minimizing flip-flop power at low data switching and to reduce redundant switching activities is to use conditional capturing [3]. Figure 10 shows the schematic of differential conditional capturing energy recovery (DCCER) flip-flop. The figs. 11 and 12 represent the simulated output and layout of DCCER respectively. The DCCER flip-flop operates in a precharge and evaluates fashion. Here precharging is done by using small pull up pMOS transistor MP1and MP2 those are always on since they are connected to ground. The DCCER flip-flop uses a NAND-based set/reset latch for the storage mechanism [3]. The output of NAND1 and NAND2 gates is connected with MN4 and MN3 transistor in the evaluation paths. If the state of the input data D and DB is having the same state as Q and QB the SET and RESET node remain as such. This results in power saving at low data switching activities or when the data remain idle for a long time.

When, three of them on simultaneously significant charge sharing may occur. One idea to reduce the charge sharing is the proper sizing of MP1 and MP2 transistor. Here MP1 and MP2 are statically on but

Figure 12. Layout of DCCER flip-flop.

they do not result in static power dissipation because as soon as Q gets the value D, the pull down path gets turned off and SET and RESET node come back in high state without any static power dissipation. The other idea is to keep the clock transistor MN1 near to ground, which is the largest transistor in evaluation path. Since, in MN1 transistor its source is near to ground so it also reduces the charge sharing to extent [3].

4.   SINGLE-ENDED   CONDITIONAL CAPTURING ENERGY RECOVERY FLIP-FLOP (SCCER)

Figure 13 shows schematic of single-ended conditional capturing energy recovery (SCCER) flip-flop. SCCER is a single-ended version of the DCCER flip-flop [3]. Here QB controls the transistor MN3 that helps to provide the conditional capturing. Only one end provides the conditional capturing. Placing MN3 above MN4, for which D is input, reduce the charge sharing. The Figs. 14 and 15 represent the simulated output and layout of SCCER flip-flop respectively.
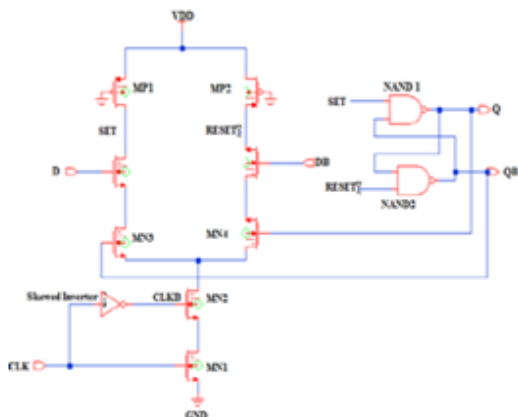

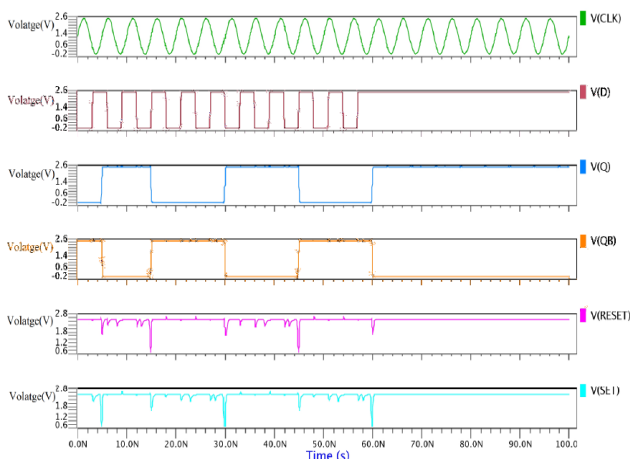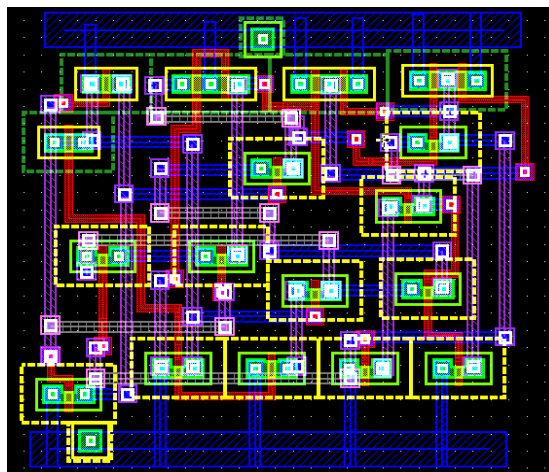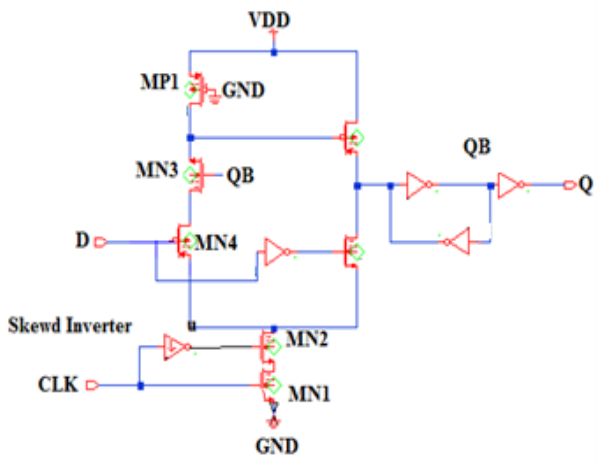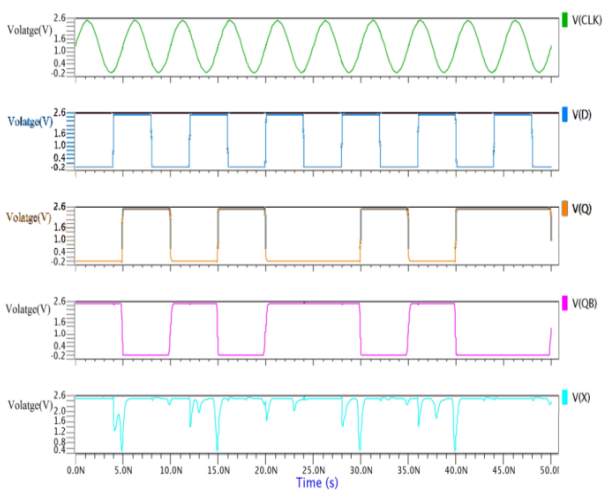Figure 10. Schematic of DCCER flip-flop.
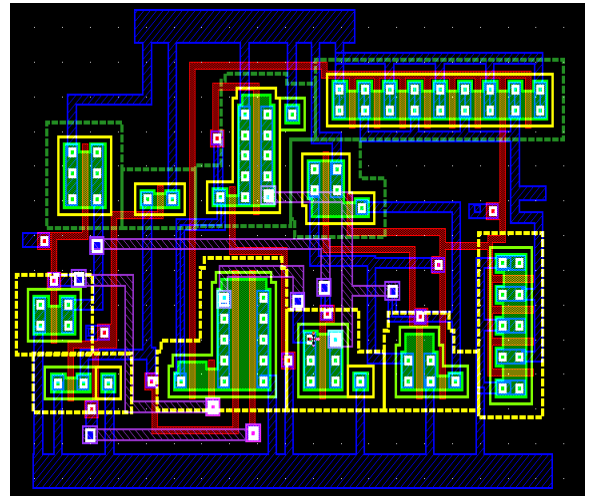

Figure 11. Simulated output of DCCER flip-flop.

To make MN1 faster we make it fairly of large size. The evaluation path consists of four transistors.

Figure 13. Schematic of SCCER flip-flop.

Figure 14. Simulated output of SCCER flip-flop.

Figure 15. Layout of SCCER flip-flop.

IV. PIPELINED MULTIPLIER

To demonstrate the functionality and accuracy of SCCER flip-flop, a 2 × 2 bit Pipelined multiplier pipelined in 3 stages is designed (figure 16). The verilog net list obtained after synthesizing (synthesized for minimum delay and area using Tsmc 0.25 µm technology) the verilog code is imported in the DA tool of Mentor graphics. Now in schematic of pipelined multiplier registers are normal D flip-flops. The input data pattern for pipelined multiplier is generated by the LFSR. It will generate the Pseudo random pattern for multiplier and all the flip-flops in multiplier are operated by 200 MHz sinusoidal clock.
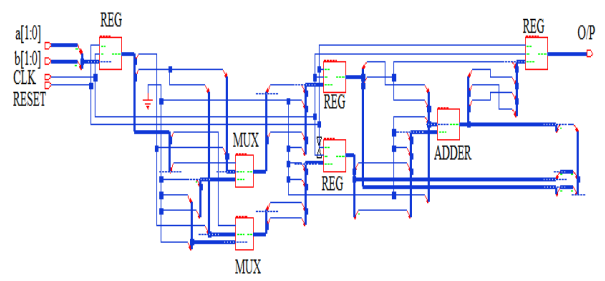

Figure 16. Schematic of 2 x 2 bit multiplier pipelined in 3 stages.

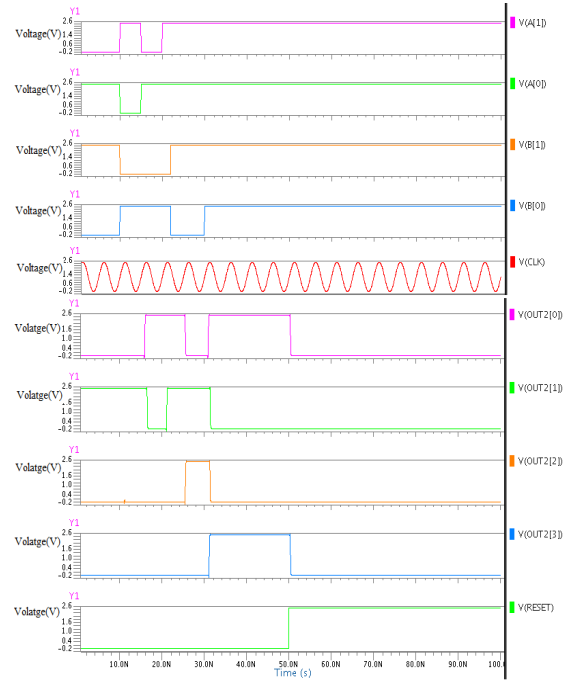### 1. PIPELINED MULTIPLIER WITH NORMAL D FLIP-FLOP

Figure 17. Simulated output of multiplier with normal D flip-flop.

The schematic obtained after importing the Verilog netlist in tool is simulated with sinusoidal clock of frequency 200 MHz generated by an efficient energy recovery clock generator [12]. Here A [1], A [0], B

[1], B [0] are the four bits inputs for multiplier generated by 4-bit LFSR. The simulated output is shown above in figure 17.

2. PIPELINED MULTIPLIER WITH SCCER FLIP-FLOP

Now we replaced all the flip-flops of pipelined multiplier with SCCER flip-flop and simulated the design. Here A [1], A [0], B [1], B [0] are the four bits inputs for multiplier generated by 4- bit LFSR. When RESET is high output is "0". When RESET is low it works as a general flip-flop and output is obtained. Since, it is a three stage pipelined multiplier so its output must be obtained at the rising edge of third clock cycle. The simulated output is shown below in figure 18.
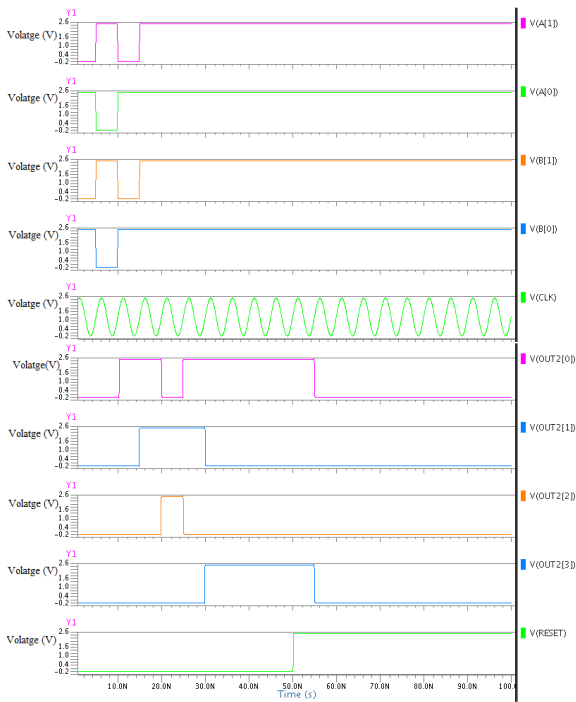

Figure 18. Simulated output of pipelined multiplier after replacing the normal D flip-flop with SCCER flip-flop.

V.   RESONANT CLOCKING

In order to demonstrate the feasibility of energy recovery clocking, we integrated 64 energy recovery clocked flip-flops distributed across an area of 1mm × 1mm and clocked them by a single-phase sinusoidal clock through an H-tree clocking network. A common data input was used for all flip-flops to easily control the data switching activity of the system. A lumped-type resistance–capacitance (RC) model for each interconnect of the clock-tree was extracted and then connected together to make a distributed RC model of the clock-tree, as shown in

figure 19 [3]. The energy recovery clock generator drives the source node of the clock-tree [node CLK in Figure 19], and each final node of the clock-tree (CLK1 to CLK16) is connected to four SCCER flip-flop (figure 20). Since the interconnect lines between each pair of nodes are assumed to be connected in parallel, the
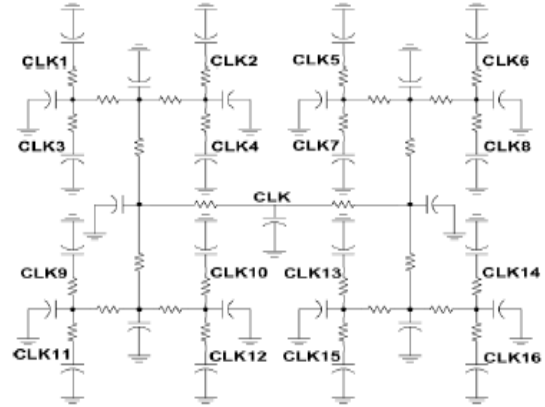

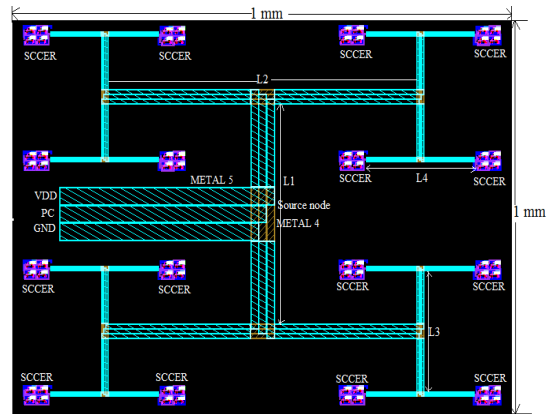Figure 19. Distributed RC model of clock tree [3].

Figure 20. 4-level deep H-tree clock network with 4 SCCER flip-flop at each node in area of 1mm × 1mm.

capacitance per unit length is increased by a factor of two, while the resistance and inductance per unit length is decreased by a factor of two at each level of the hierarchy [2]. The design methodologies [2, 17] are used to design the clock network with minimum skew. Metal-5 and metal-4 layer are used to form the clock network since it has the smallest parasitic capacitance and resistance to substrate which is the limiting factor in the distribution of the clock. In Tsmc 0.25 μm technology the maximum metal width of metal-5 is 35 μm to be used to reduce the parasitic resistance. The width of the metal wire becomes half at each node for impedance matching while the separation is same. The wider wires also follow the minimum skew. The total covered length

of metal-5 layer in our work is 5000 μm. The separation between each wire is s = 1 μm. A lumped type ∏- RC model is form after extracting the RC value from the .PEX net list for each component of wire. The following figure 21 represents the simulated output of SCCER flip-flop in H- tree clock network.
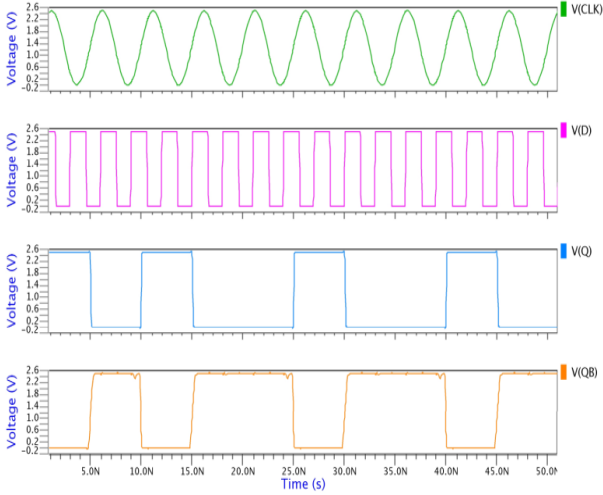

Figure 21. Simulated output of SCCER flip-flop in H-tree clock network.

VI. ANALYSIS AND OBSERVATIONS

Table 1 shows the calculated value of SAER, SDER, DCCER and SCCER flip-flop in terms of min D-Q delay, set up time, hold time, CLK-Q delay, total power dissipation and PDP. These values are similar to the values reported earlier (Mahmoodi et al., 2009). Further, It can be seen from table 1., that SCCER flip-flop shows the best performance in terms of PDP and CLK-Q delay parameters, among all the flip-flops. Further figure 22 shows the bar chart of PDP for all flip-flops for switching activity at α = 0.5. It can be seen from figure 22 that SCCER flip-flop has the lowest value of PDP which is similar to the values reported in literature (Mahmoodi et al., 2009). This lowest value of PDP for SCCER flip-flop shows the efficiency of conditional capturing. Moreover, CLK-Q delay for various flip-flops has been studied for switching activity at α = 0.5.

Figure 23 shows the bar chart of CLK-Q delay of SAER, SDER, DCCER and SCCER flip-flop for switching activity α = 0.5. Form figure 23 it can be noticed that the SCCER flip-flop has the lowest CLK-Q delay. It is important to note here that for SCCER flip-flop, both PDP and CLK-Q have lowest values comparative to other flip-flops. Since the

values of PDP and CLK-Q parameters is lowest for SCCER flip-flop so here we have investigated the functionality of SCCER flip-flop in pipelined multiplier and compare with D flip-flop.
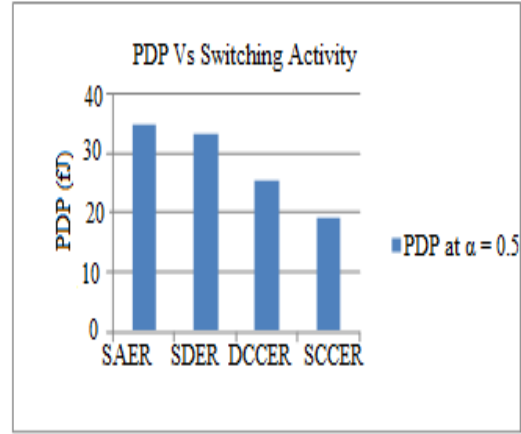

Figure 22. Represents PDP at α = 0.5 for f = 200MHz.

Table 2 shows the numerical results of the power dissipated on the clock tree, the percentage of energy recovered from the clock network by the conventional flip-flop (HLFF) and energy recovery clocked flip-flops. The clock tree capacitance shown includes the wiring capacitance of the clock network and the gate capacitance shown by the flip-flop clock inputs. The energy recovered by the SCCER flip-flop in the clock network by using 64 flip-flops is ≈ 90% with respect to conventional flip-flop (HLFF).
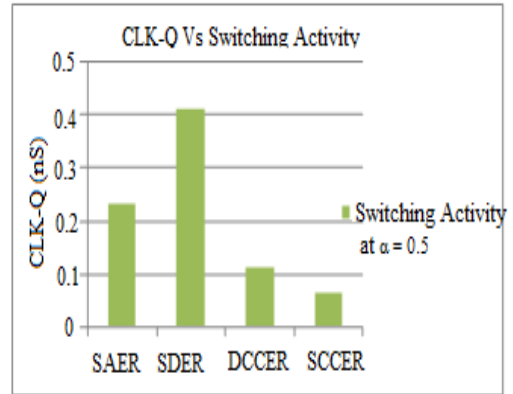

Figure 23. Represents CLK-Q delay at α = 0.5 for f = 200MHz.

Table 3 shows the comparison of total power dissipated in a multiplier (power dissipated by LFSR and resonant clock generator is excluded) with normal D flip-flop and SCCER flip-flop. For both the cases sinusoidal clock of 200 MHz is used.

Table 1. Summary of numerical results of all the energy recovery flip-flops.

Flip-Flops	Min D-Q delay (nS)	Set up (nS)	Hold (nS)	CLK-Q delay (nS)	Power(µ watt)	PDP*(fJ)	Transistor count (without inverter)	Total width (µM)
SAER	0.53	0.58	1.48	0.23	65.3	34.61	18	22.1
SDER	0.41	0.25	1.3	0.41	80.2	32.88	14	9.3
DCCER	0.37	1.6	0.76	0.11	68.4	25.31	18	25.26
SCCER	0.38	0.32	1.72	0.065	49.93	18.97	17	37

Table 2. Comparison of power dissipated in clock network using conventional flip-flop (HLFF) and SCCER flip-flop.

Flip-flop	No. of flip-flop	Clock	Clock tree power [mW]	Clock tree cap. [pF]	Clock power/pF load [mW/pF]	Energy recovery (%)
Conventional flip-flop (HLFF)	64	Square wave	30.52	24.42	1.25	0
SCCER flip-Flop	64	Sinusoidal clock of single phase	5.12	40	0.128	89.76

Table 3. Represents the comparison of total power dissipated in a multiplier with normal D flip-flop and SCCER flip-flop.

Pipelined multiplier	Number of transistors used in flip-flops	Total Power dissipation (Miliwatt)
D flip-flop	18	2.0843
SCCER flip-flop	17	1.1763

It can be seen that the use of SCCER flip-flop in the pipelined multiplier dissipates 43.56% less power against the normal D flip-flop. The less number of transistors in SCCER flip-flop makes it compact in terms of area.

CONCLUSION

Thus energy recovery is best scheme to recover the energy from a highly capacitive clock network. The SCCER flip-flop dissipates 43.56% less power in a pipelined multiplier in compare of normal D flip-flop. There is 90% energy recovery in case of SCCER flip-flop with respect to conventional flip-flop (HLFF) that operates with square wave clock.

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